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(54) Title: CDMA COMMUNICATION SYSTEM IN WHICH BIT RATES ARE DYNAMICALLY ALLOCATED

(57) Abstract

A CDMA communication system is provided in which bit rates are dynamically allocated by a single CDMA receiving station (RS) to a plurality of CDMA transmitting stations, (TS₁, TS₂ ...) all of which are intercoupled to each other over a CDMA channel (FB₁) and a feedback channel (FB₂). Each CDMA transmitting station (Fig.3) includes a control circuit (31, 32) which sends control signals (Fig. 2A) on the CDMA channel in spaced apart time intervals which request respective bit rates on the CDMA channel; and, the CDMA receiving station (Fig. 4) includes a bit rate allocating circuit (52, 53, 54) which receives and responds to the control signals by sending feedback messages (Fig. 2B) over the feedback channel that address individual CDMA transmitting stations and grant respective bit rates to the addressed station. In one preferred embodiment, each transmitting station includes a data buffer (30) which stores a time varying number of data bytes that are to be sent, and each transmitting station requests respective bit rates on the CDMA channel by including that number in the control signals.

CDMA COMMUNICATION SYSTEM IN WHICH BIT RATES
ARE DYNAMICALLY ALLOCATED

BACKGROUND OF THE INVENTION:

This invention relates to communication systems;
and more particularly, it relates to multipoint-to-point
CDMA communication systems.

5   As used herein, the term "multipoint-to-point"
refers to a communication system in which multiple
transmitting stations, which are located at respective
points, simultaneously send separate data blocks to a
single receiving station which is located at one other
10 point.   That is, a first data block is sent by a first
transmitting station, a second data block is sent by a
second transmitting station, etc.; and, any number of these
data blocks can be sent at the same time.

One way to operate such a system is to have each
15 transmitting station send its data as an amplitude
modulated signal in its own wireless channel which differs
in frequency for each transmitting station.   However, if
the total number of transmitting stations in the
communication system is large, then a corresponding large
20 number of separate frequency bands is required.
Alternatively, each transmitting station can send its data

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over a separate optical fiber to the receiving station.
However, when the receiving station is remotely located
from the transmitting stations, too much connecting optical
fiber is required.

5   By comparison, with a multipoint-to-point CDMA
communication system, all of the transmitting stations send
their data in either a single wireless channel or a single
optical fiber. By the term "CDMA" is herein meant "Code
Division Multiple Access."   In a CDMA system, each
10 transmitting station encodes the data that it sends with a
respective spreading code which is unique to that station.
Then, the encoded data from all the transmitting stations
is sent simultaneously on a single wireless channel/optical
fiber in one frequency band to the receiving station.

15   In the receiving station, the data from any one
particular transmitting station is recovered by exclusive-
oring the composite CDMA signal with the same spreading
code which was used to encode the data. One prior art CDMA
receiving station is described in U.S. Patent 4,908,836 by
20 Rushforth, et al.,   entitled "Method and Apparatus for
Decoding Multiple Bit Sequences That Are Transmitted
Simultaneously in a Single Channel". Also, another CDMA
receiving station is described in U.S. Patent 5,031,173 by
Short, et al., entitled "Decoder for Added Asynchronous Bit
25 Sequences".   Both of these patents are assigned to the
assignee of the present invention.

           In the prior art, each transmitting station can
have a first-in-first-out data buffer (FIFO data buffer)
which temporarily holds the data that is to be transmitted.
30 With a FIFO data buffer, the data that is to be transmitted
is written into the buffer from an external source at one
bit rate, while simultaneously, data is read from the
buffer and transmitted to the receiving station at a
different bit rate. Consequently, if the rate at which
35 data is written into the buffer exceeds the rate at which
data is read from the buffer during a long time period,

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then an overload condition can occur wherein the storage capacity of the data buffer is exceeded.

Also, in the prior art, the number of stations which actually transmit CDMA data at any one time instant can vary greatly. For example, suppose that the CDMA communication system includes 100 different transmitting stations. In that case, the number of transmitting stations which actually transit CDMA data at the same time instant can vary from 1 to 100. Thus, when each transmitting station sends its data at a fixed bit rate, then a dilemma occurs. If the bit rate of each transmitting station is set high, the total bit rate capacity of the CDMA network can be exceeded whenever a large numbered stations are actually transmitting. But if the bit rate of each transmitting station is set low, then a buffer overload can frequently occur.

Accordingly, a primary object of the present invention is to provide an improved multipoint-to-point communication system in which the above drawbacks are overcome.

BRIEF SUMMARY OF THE INVENTION:

With the present invention, a CDMA communication system is provided in which bit rates are dynamically allocated. This CDMA communication system includes a plurality of CDMA transmitting stations and a single CDMA receiving station, all of which are intercoupled to each other over a CDMA channel and a feedback channel. Each CDMA transmitting station includes a control circuit which sends control signals on the CDMA channel in spaced apart time intervals which request respective bit rates on the CDMA channel; and, the CDMA receiving station includes a bit rate allocating circuit which receives and responds to the control signals by sending feedback messages over the feedback channel that address individual CDMA transmitting stations and grant respective bit rates to the addressed

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station. Each CDMA transmitting station receives those
feedback messages which have its address, and each CDMA
transmitting station sends CDMA data on the CDMA channel at
the bit rates granted in the received feedback messages.

In one preferred embodiment, each transmitting
station includes a data buffer which stores a time varying
number of data bytes that are to be sent, and the
transmitting station requests respective bit rates on the
CDMA channel by including that number in the control
signals. Also in one preferred embodiment, each CDMA
transmitting station encodes its data with a spreading code
at a fixed number of chips per second and a selectable
number of chips per bit in response to the granted bit
rate. Further, in one preferred embodiment, the bit rate
allocating circuit tallies the bit rates which it grants in
the feedback messages, and it maintains that tally below
a predetermined maximum aggregate bit rate for the CDMA
channel.

BRIEF DESCRIPTION OF THE DRAWINGS:

Fig. 1 shows an overview of a CDMA communication
system which constitutes one preferred embodiment of the
present invention.

Fig. 2A shows a format for CDMA signals which are
sent by several CDMA transmitting stations in the Fig. 1
communication system.

Fig. 2B shows a format for feedback messages
which are sent by one CDMA receiving station to several
CDMA transmitting stations in the Fig. 1 communication
system.

Fig. 3 is a detailed circuit diagram of a
preferred embodiment for each CDMA transmitting station in
Fig. 1.

Fig. 4 is a detailed circuit diagram of a
preferred embodiment for the CDMA receiving station in
Fig. 1.

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Fig. 5 shows a preferred embodiment of a bit rate allocation program which is executed by the CDMA receiving station in Fig. 4.

Fig. 6 is a timing diagram which illustrates a sequence by which the CDMA transmitting stations and CDMA receiving station in Fig. 1 change the bit rate at which they respectively transmit and receive data.

DETAILED DESCRIPTION:

Referring now to Fig. 1, a CDMA communication system which constitutes one preferred embodiment of the present invention will be described. This Fig. 1 embodiment includes a plurality of CDMA transmitting stations TS_1, TS_2, TS_3, . . . etc.; and it includes a single CDMA receiving station RS. All of the CDMA transmitting stations and the single CDMA receiving station are interconnected to each other by a single coaxial cable 10 as shown.

Suitably, the coaxial cable 10 is a pre-existing cable in a conventional cable television network. In that case, the cable 10 carries standard cable television signals which in Fig. 1 are labeled TV; the CDMA transmitting stations are located in respective houses which receive the TV signals; and the CDMA receiving station is located in the cable television plant which supplies the TV signals. All of the TV signals occur in a frequency band FB_0, and they are not used by the CDMA transmitting stations or the CDMA receiving station.

Each CDMA transmitting station TS_i operates by sending signals $CDMA_i$ over the cable 10 to the receiving station RS. That is, station TS_1 sends signals $CDMA_1$; station TS_2 sends signals $CDMA_2$; etc. Any number of these signals can occur on the cable 10 simultaneously whereupon they are added together to form a composite signal CDMA. Each of the signals $CDMA_1$, $CDMA_2$, etc., fully occupy the

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same frequency band FB_1 which is separate from the frequency band FB_0.

In response to each of the $CDMA_i$ signals, the receiving station RS sends a feedback message M_i on the cable 10 back to the corresponding transmitting station TS_i. These feedback messages occur in a frequency band FB_2 which is separate from the frequency bands FB_0 and FB_1. Since the three frequency bands FB_0, FB_1, and FB_2 are all separate from each other, the corresponding TV signals and CDMA signals and feedback messages M_i can all occur on the cable 10 at the same time without interfering with each other.

Fig. 2A shows a preferred format for each of the signals $CDMA_i$; and Fig. 2B shows a preferred format for each of the feedback messages M_i. In Fig. 2A, each of the $CDMA_i$ signals includes a header 20 that is followed by a block of data 21, which is a fixed number of data bits. This header 20 identifies a destination 20a to which the data 21 is forwarded over a network 11 by the receiving station RS. Network 11 can be any conventional communication network, such as a telephone network.

Also, the header 20 includes a count 20b; and this count constitutes a request by the transmitting station TS_i to send its data 21 at a certain bit rate. Specifically, when the count is high, the count constitutes a request to transmit data at a correspondingly high bit rate; whereas when the count is low, the count constitutes a request to transmit data at a correspondingly low bit rate. Preferably, each transmitting station TS_i includes a first-in-first-out data buffer which stores a time varying number of data bytes that are to be sent. In that case, the count 20b which is sent in the header equals the number of data bytes that are stored in the data buffer.

Within the receiving station RS, the count 20b in each of the $CDMA_i$ signals is received. Then, in response to the count CNT_i, the receiving station RS sends the feedback messages M_i over the cable 10 which address the CDMA

transmitting station TS_i and grants a particular bit rate to
the addressed station. This is shown in Fig. 2B wherein
each message M_i includes a header 25; and that header may,
or may not, be followed by a block of data 26. In the
5 header 25, an address A_i is included which addresses a
particular CDMA transmitting station TS_i. Also in the
header 25, a bit rate BR_i is included which is granted to
the addressed transmitting station.

       In one preferred embodiment of the CDMA receiving
10 station which will be described shortly in conjunction with
Fig. 4, a microprocessor is included which tallies the bit
rates that are granted in the feedback messages M_i. By
keeping this tally, the CDMA receiving station RS is able
to grant bit rates in the messages M_i which maintain the
15 total bit rate for all of the $CDMA_i$ signals below a
predetermined maximum aggregate bit rate BR_{max}.

       For example, suppose the maximum aggregate bit
rate for all of the $CDMA_i$ signals on the cable 10 is ten M_{bps}
(10 megabits per second); and suppose further that only
20 three stations TS_1, TS_2, and TS_3 have data to transmit. In
that case, at one time instant, the respective bit rates
which are granted to the transmitting stations TS_1, TS_2 and
TS_3 could be 1 Mbps, 2 Mbps and 6 Mbps. Thereafter, due to
a change in the count signals CNT_i, the respective bit rates
25 which are granted could be 5 Mbps, 1 Mbps, and 4 Mbps.

       Suitably, the maximum aggregate bit rate BR_{max} is
set at about 90 percent of a bit rate at which errors start
to occur in the data that is recovered by the receiving
station RS. This leaves about 10 percent of the aggregate
30 bit rate for any stations TS_i which are not currently
transmitting $CDMA_i$ signals to start their transmissions.

       Turning now to Fig. 3, a preferred internal
structure for each of the CDMA transmitting stations TS_i
will be described. This Fig. 3 embodiment includes several

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electronic modules 30-41; and each of these modules is
identified below in Table 1.

TABLE 1

MODULE   DESCRIPTION

30...... A first-in-first-out data buffer (FIFO)
          which receives data on an input 30a and
          sends data on an output 30b. This data
          buffer generates the count signal CNT_i,
          on an output 30c, equal to the number
          of data bytes that are stored in the
          data buffer.

31...... A microprocessor, such as a Motorola
          680X0 chip, including an associated
          instruction memory.

32...... A register which holds the header 20 of
          the signals $CDMA_i$.

33...... A 2 x 1 multiplex.

34...... A spreading code generator which
          generates a spreading code PN_i on an
          output 34a.

35...... An exclusive-or logic gate which
          exclusive-or's signals from the
          multiplexer 33 with the spreading code
          PN_i from the generator 34 and sends the
          result to an output 35a.

36...... A modulator circuit which generates, on
          the cable 10, a frequency shifted
          replica of the output signals from the

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exclusive-or gate 35. This frequency
shifted signal is signal $CDMA_i$ in the
frequency band FB_1.

37...... A pair of filters, one of which passes
the messages M_i in the frequency band
FB_2 from the cable 10 to output 37a,
and another which passes the television
signals TV in the frequency band FB_0 to
output 37b.

38...... A message selecting circuit which
examines the address in each message M_i
and passes only those messages which
have the address A_i that is assigned to
the particular transmitting station
TS_1.

39...... A first-in-first-out data buffer (FIFO)
which stores data from circuit 38 when
that data is preceded by a header which
contains address A_i.

40...... A chip clock generator which generates
a clock signal CK at a fixed frequency
which equals the chip rate of the
spreading code (i.e. signal CK is 10
MHz if the chip rate is 10 million
chips per second).

41...... A control circuit which responds to
commands from the microprocessor 31.
Each command selects the number of
chips in the spreading code which
encode a single bit of transmitted
data.

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Likewise, a preferred internal structure for the CDMA receiving station is shown in Fig. 4. This Fig. 4 embodiment includes several electronic modules 50-57; and each module is identified below in Table 2.

5   **TABLE 2**

MODULE	DESCRIPTION
50......	A filter which receives all of the signals on the cable 10, and which passes to an output 50a just the CDMA signals in frequency band FB_1.
51-1.... thru 51-N	Each of these is a CDMA receiver module. Module 51-i locks onto the spreading code PN_i in the composite CDMA signal from the cable 10. After locking, module 51-i recovers the header 20 and the data 21 which is in the $CDMA_i$ signal. All of the data 21 along with the destination 20a in the header is passed to an output 51a-i; whereas the count 20b in the header is passed to an output 51b-i.
52......	A microprocessor, such as a Motorola 680X0 chip.
53......	A memory in which a bit rate allocation program is stored. One preferred embodiment of this program is shown in Fig. 5. Execution of this program by the microprocessor 52 generates the bit rate signals BR_j.

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54...... A memory which stores several
parameters that are used by the bit
rate allocation program in memory 53.

55...... A message formatting circuit which
receives the bit rate signals BR_i on
output 52a from the microprocessor 52,
and which formats them along with any
data block 26 as the messages M_i on
output 55a.

56...... A modulator circuit which receives the
messages M_i from circuit 55 and
replicates them on the cable 10 in the
frequency band FB_2.

57...... A circuit which receives the television
signals TV from an external source and
passes those signals to the cable 10 in
frequency band FB_0.

In operation, all of the electronic modules 30-41
of the Fig. 3 CDMA transmitting station TS_i and all of the
electronic modules 50-57 of the Fig. 4 CDMA receiving
station RS interact with each other as follows. Initially,
when data is to be transmitted by the Fig. 3 transmitting
station, the destination 20a for the data is sent to the
microprocessor 31 on an input 31a. Thereafter, the data 21
which is to be transmitted is sequentially loaded one byte
at a time into the data buffer 30 via the data buffer input
30a. This data 21 along with its destination 20a can come
from any external module, such as a home computer.

As each data byte is loaded, the count signal CNT_i
on the data buffer output 30c is incremented by one; and
this count signal is sensed by the microprocessor 31. When
the count signal CNT_i indicates that the data buffer 30

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stores at least a certain minimum number of data bytes
(e.g. 32 data bytes), the microprocessor 31 generates the
header 20 by sending the destination 20a and the count 20b
on an output 31b to register 32. Then, to start
5   transmitting the CDMA$_i$ signals, the microprocessor 31 sends
a command on a output 31c to the control circuit 41. This
command specifies the number of chips of spreading code PN$_i$
which encode each bit of the CDMA$_i$ signals; and initially it
is set a predetermined number.
10   Control circuit 41 responds to the command by
sending several control signals on its outputs 41a-41d.
The control signals on output 41a direct the generator 34
to start generating the spreading code PN$_i$ on output 34a.
The control signals on output 41b direct the multiplexer 33
15 to pass either the header from register 32 or the data from
data buffer 30 to the modulator 35. The control signals on
output 41c cause the header to be read bit-by-bit from the
register 32. And the control signals on output 41d cause
the data words to be read bit-by-bit from the data buffer
20 30 and cause the count signals CNT$_i$ to be decremented by one
each time a byte of data is read.
            Each bit of the header from register 32 and each
bit of the data from the data buffer 30 which passes
through the multiplexer 33 to the logic gate 35 is
25 exclusive-or'd with several chips of the spreading code PN$_i$.
The number of chips per bit is determined by the command
which microprocessor 31 sent to the control circuit 41.
Then, the encoded signals on output 35a go to circuit 36
where they are shifted into the frequency band FB$_1$. This
30 generates the CDMA$_i$ signals which travel on the cable 10 to
the Fig. 4 receiving station.
            In the receiving station of Fig. 4, the CDMA$_i$
signals pass through the FB$_1$ filter 50 to the CDMA receiver
modules 51-1 through 51-N. Module 51-i locks onto the
35 spreading code PN$_i$ in the composite CDMA signal from the
filter output 50a; and module 51-i then recovers the header

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20 and the data 21 which is in the $CDMA_i$ signal. Suitably,
in order to perform this operation of recovering the header
20 and the data 21 in the $CDMA_i$ signal, each read module 51-
1 through 51-N has an internal structure as disclosed in
5   U.S. patents 4,908,836 and 5,031,173 which are assigned to
the assignee of the present invention.

All of the data 21, as well as its destination
20a, which is recovered by the read module 51-i is
presented on an output 51a-i. From that output, the data
10 21 is forwarded to its destination 20a in a conventional
fashion, such as by a modem over the telephone network 11
in Fig. 1. Conversely, the count signal CNT_i which is
recovered by the read module 51-i is sent on an output 51b-
i to the microprocessor 52.

15   Each time the microprocessor 52 receives one of
the count signals CNT_i, the microprocessor grants a
corresponding bit rate BR_i. To generate this BR_i signal, the
microprocessor 52 executes the bit rate allocation program
which is stored in memory 53; and one preferred embodiment
20 of the bit rate allocation program will be described
shortly in conjunction with Fig. 5.

During the execution of the bit rate allocation
program, several parameters are utilized which are stored
in memory 54. Those parameters are labeled in Fig. 4 as
25 $LCNT_i$, LBR_i, $LEBR_i$, and $LABR_i$. Parameter $LCNT_i$ is the last
value of the count signal CNT_i which was recovered by the
read module 51-i. Parameter LBR_i is the corresponding last
bit rate which was granted in response to the last count
signal. Parameter $LEBR_i$ is the last estimate of a minimum
30 bit rate which station TS_i needs to insure that its data
buffer 30 does not overflow. One such estimate is made by
the microprocessor 52 for each count signal CNT_i which it
receives. Parameter $LABR_i$ is a running average of the
parameter $LEBR_i$ as it is generated for station TS_i over time.

35   Each bit rate signal BR_i which is generated by the
microprocessor 52 is sent back to the read module $RMOD_i$ and

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to circuit 55. Module $RMOD_j$ stores the bit rate BR_j for
later use, whereas circuit 55 immediately uses the bit rate
signals BR_j to form the header 25 which was previously
described in conjunction with Fig. 2B. Also, circuit 55
5   appends to the header, a block of data 26 whenever that
block has been received on input 55b for the same CDMA
transmitting station which is to receive the bit rate
signals BR_j. Then, the header 25 (and any appended data 26)
is sent by circuit 55 on an output 55a to the modulator
10 circuit 56. That circuit 56 replicates the header 25 and
data 26 on the cable 10 in the frequency band FB_2; and each
such replication constitutes a feedback message M_j.

        Feedback message M_j travels on the cable 10 to the
CDMA transmitting station TS_j whereupon it goes through the
15 FB_2 filter 37 to the filter output 37a. Then, circuit 38
examines the address A_j in the message M_j. If the address A_j
matches an address which is preassigned to the transmit
station TS_j, the corresponding bit rate signal BR_j is sent
on an output 38a to the microprocessor 31. Also, if the
20 address A_j matches the address for the transmit station TS_j,
then any data 26 which follows the header is sent by
circuit 38 on an output 38b to the data buffer 39.
Thereafter, the data which is stored in the buffer 39 is
read by an external module, such as a home computer.

25   Each bit rate signal BR_j on output 38a is read by
the microprocessor 31; and in response, the microprocessor
31 converts the received bit rate BR_j to a corresponding
chips-per-bit command. If the received bit rate BR_j is
high, the corresponding command specifies a small number of
30 chips per bit; and vice versa. Command #1 selects X chips
per bit; command #2 selects X + 1 chips per bit; . . .
command #N selects X + N -1 chips per bit. Preferably, X
is an integer in the range of sixteen to two-hundred fifty-
six.

35   Then, the microprocessor 31 sends the command
which specifies the new chip-per-bit ratio on its output

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31c . In response, at the start of the next header, the
control circuit 41 changes the control signals on its
outputs 41a-41d such that the $CDMA_i$ signals are transmitted
with the new chip-per-bit ratio. Thereafter, the entire
5   sequence as explained above repeats over and over again.

            One preferred structure for the bit rate
allocation program 53 which is executed by the CDMA
receiving station is shown in Fig. 5. This Fig. 5 program
consists of a set of steps 70 through 77, each of which
10 will now be described.

            In step 70, an estimate is made of the minimum
bit rate which station TS_i needs in order to insure that its
output data buffer 30 does not overflow. This estimated
bit rate EBR_i is determined as a predetermined function
15 f( ) of the parameters CNT_i, $LCNT_i$, $LEBR_i$, and $LABR_i$. All of
those parameters are read by the microprocessor 52 from the
memory 54. By this function f( ), the estimated bit rate
EBR_i will increase over the last estimated bit rate $LEBR_i$
whenever the count signal CNT_i is too high and/or is
20 continually increasing. Conversely, the estimated bit rate
EBR_i will decrease over the last estimated bit rate $LEBR_i$
whenever the count signal CNT_i is very low and/or is
continually decreasing.

            Next, in step 71, the running average ABR_i of the
25 estimated bit rates EBR_i is updated by the expression $k_1 BR_i$
+ $k_2 LABR_i$. Here, the terms k_1 and k_2 are constants which,
for example, may respectively be 0.2 and 0.8. Also in step
71, the unused aggregate bit rate UBR for the CDMA channel
is determined by evaluating the expression $BR_{max} - \Sigma LBR$.
30 This unused aggregate bit rate UBR is the peak amount by
which the last bit rate LBR_i can be increased without
exceeding the capacity of the CDMA channel.

            Next, step 72 is performed wherein a test is made
to determine whether the estimated EBR_i is an increase or a
35 decrease over the last bit rate LBR_i that was granted to
station TS_i. If the estimated bit rate EBR_i is an increase

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over the last bit rate LBR_i, then step 73 is performed.
Otherwise, step 74 is performed.

In step 73, a new bit rate BR_i for station TS_i is
set to the estimated bit rate EBR_i provided that the maximum
5 aggregate bit rate BR_{max} for the CDMA channel will not be
exceeded. If that maximum aggregate bit rate BR_{max} would
be exceeded, then the new bit rate BR_i for station TS_i is set
to the last granted bit rate LBR_i plus the unused aggregate
bit rate UBR.

10 In step 74, the new bit rate BR_i is set to one of
three difference values. If the estimated bit rate EBR_i is
larger than the running average bit rate ABR_i and less than
the unused aggregate bit rate UBR_i, then the new bit rate BR_i
is set equal to EBR_i. If the running average bit rate ABR_i
15 is larger than the estimated bit rate EBR_i and less than the
unused aggregate bit rate UBR, then the new bit rate BR_i is
set equal to ABR_i. Otherwise, the new bit rate BR_i is set
equal to the unused aggregate bit rate UBR.

Next, in step 75, the magnitude of the difference
20 between the new bit rate BR_i and the last granted bit rate
LBR_i is compared to a threshold ϵ. If that threshold is
exceeded, then step 76 is performed wherein a message is
sent on the feedback channel which grants the new bit rate
BR_i to the CDMA transmitting station TS_i. Also, in step 76,
25 the parameter LBR_i is updated in the memory 54 with the
newly granted bit rate BR_i.

Conversely, if the threshold ϵ is not exceeded,
then step 76 is bypassed. In that case, the bit rate in
the transmitting station TS_i remains unchanged. As a
30 result, small bit rate changes are suppressed; and this
minimizes the number of messages which are sent on the
feedback channel thereby reducing overhead.

Lastly, in step 77, the parameters $LEBR_i$, $LABR_i$,
and $LCMT_i$ are updated in the memory 54. Parameter $LEBR_i$ is
35 set equal to the estimated bit rate EBR_i as determined in

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step 70; parameter $LABR_i$ is set equal to the running average
bit rate ABR_i as determined in step 71; and the parameter
$LCMT_i$ is set equal to the count signal CMT_i which was just
processed.

5   Turning now to Fig. 6, it provides a timing
diagram which illustrates how the bit rate changes are
synchronized between the transmitting station TS_i and the
receiving station RS. This timing diagram includes several
signal waveforms that have reference numerals 80 through
10 86; and each of these waveforms is described below.

          Waveform 80 shows the signal $CDMA_i$ at the transmit
station TS_i. By comparison, waveform 81 shows the signal
$CDMA_i$ in the receive station RS at the read module $RMOD_i$.
Waveform 81 is a delayed replica of waveform 80 due to an
15 inherent time delay which is caused by the cable 10.

          Both of the waveforms 80 and 81 as shown in Fig.
6 begin at a time t_0 which occurs when the $CDMA_i$ signal is
transmitting the data 21. Prior to time t_0, the header 20
was transmitted; and waveform 82 shows the feedback message
20 M_i as it is sent at the station RS in response to the count
CNT_i which is in the header. That message M_i begins in
station RS at a time t_1; and it includes the new bit rate
BR_i which is granted to the transmit station TS_i.

          Waveform 83 shows the feedback message M_i as it is
25 received at the transmit station TS_i. Here again, waveform
83, which begins at time t_2, is a delayed replica of
waveform 82 due to the inherent delay that is caused by the
cable 10.

          Waveform   84   shows   the   command   which
30 microprocessor 31 in the transmit station TS_i sends to the
control circuit 41 in response to the feedback message M_i.
This command begins at a time instant t_3, and it specifies
the new number of chips which will encode each bit in the
$CDMA_i$ signal.

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This new chip-per-bit ratio which is specified by the command of waveform 84 does not take effect immediately. Instead, that chip-per-bit ratio takes effect in the transmitting station TS_i when the next header starts
5 to get transmitted. This is illustrated in Fig. 6 by waveforms 80 and 85.

Waveform 85 is timing pulse which begins at time t_4. This timing pulse is generated within control circuit 41 of the transmit station TS_i by counting the number of
10 data bits which are read from the buffer 30 and transmitted after each header, and by generating waveform 85 when a complete block of data 21 has been sent.

Likewise, in the receive station RS, the new bit rate BR_i takes effect when the next header begins to be
15 received by the read module $RMOD_i$. This is illustrated in Fig. 6 by waveforms 81 and 86. Waveform 86 is a timing pulse that begins at a time t_5, which is when the next header starts being received. This timing pulse is generated within the read module $RMOD_i$ by counting the
20 number of data bits which are received after a header, and by generating waveform 86 when a complete block of data 21 is received.

For each count signal CNT_i that is sent by the transmitting station TS_i, the entire signal sequence which
25 occurs during times t_0-t_5 in Fig. 6 is repeated. This is indicated in Fig. 6 by waveform 80 at time t_0'. At that time, more data 21 is again starting to be transmitted after the transmission of a header. Thus, time t_0' corresponds to the preceding time t_0.
30 One primary feature of the above-described CDMA communication system is that it prevents the data buffer 30 in the CDMA transmitting station from becoming overloaded. This feature occurs because as the data buffer 30 fills up, the count signal CNT_i on output 30c will increase; and that
35 count signal CNT_i is sent to the CDMA receiving station. If the count signal CNT_i is high or increasing at a high rate,

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then microprocessor 52 will grant a correspondingly high
bit rate BR_i back to the transmitting station TS_i. There,
microprocessor 31 will cause the high bit rate BR_i to take
effect by sending a command to the control circuit 41 which
5 decreases the number of spreading code chips in each bit of
the $CDMA_i$ signals.

        Also, another primary feature of the above-
described CDMA communications system is that the total bit
rate of all of the $CDMA_i$ signals on the cable 10 is
10 maintained below a maximum aggregate bit rate BR_{max} for the
channel.   This is achieved by the bit rate allocation
program 53 in the receiving station RS which tallies the
bit rates that are granted to all of the transmitting
stations.   This sum of the granted bit rates is then
15 compared to BR_{max}, and each new bit rate BR_i is selected
such that the sum does not exceed BR_{max}.

        One preferred embodiment of a CDMA communication
system which is structured according to the present
invention has now been described in detail. In addition,
20 however, many changes and modifications can be made to
these details without departing from the nature and spirit
of the invention.

        As one such modification, the cable 10 can be
replaced with any other media which carries the CDMA
25 signals and the feedback messages M_i. For example, the
cable 10 can be replaced with a hybrid optical fiber-
coaxial cable transmission medium.   Alternatively, the
cable 10 can be replaced with a wireless transmission
medium.

30   As another modification, the number of data bits
in the data block 21 of the signals $CDMA_i$ can be variable.
One way to implement this modification is to include a
field in the header 20 before the data block which
specifies the number of data bits that follow. Similarly,
35 the number of data bits in the data block 26 of the
feedback messages M_i can be a variable.

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As another modification, the count signal CNT_i which occurs in the header 20 of Fig. 2A can be replaced with the change in the count ΔCNT_i which occurs between successive headers. This term ΔCNT_i can be generated by the microprocessor 31 in each transmitting station simply by subtracting each count from the preceding count. Similarly, the CDMA receiving station can use the term ΔCNT_i to determine the count CNT_i for use in the bit rate allocation program, simply by adding successive ΔCNT_i terms together.

As another modification, the bit rates BR_i which are granted in the feedback messages M_i may be generated by any process which can be performed by the microprocessor 52 in the CDMA receiving station, and not just the illustrated steps of Fig. 5. For example, step 74 of the Fig. 5 process can be modified to include a test for the case where the unused aggregate bit rate UBR is essentially zero. If such a case occurs, a feedback message can be sent to a different CDMA transmitting station TS_x which reduces that station's current bit rate LBR_x by an amount ΔBR_x. Then, the bit rate for station TS_i can be set to LBR_i plus ΔBR_x.

Also, as another modification, each CDMA transmitting station TS_i can implement the respective bit rates which it is granted by keeping the number of chips per bit fixed and varying the number of chips per second from the PN generator 34. With this modification, the number of chips per second from the PN generator 34 will increase as the bit rate which is granted by the signals BR_i increases; and vice versa.

Also, as another modification, each CDMA transmitting station can send its count signals CNT_i and its digital data signals at the same time. With this modification, each transmitting station TS_i will include two different spreading code generators 34. One such generator

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is used to encode the count signals, while the other
generator is used to encode the data from the data buffer.
Accordingly, it is be understood that the present
invention is not limited to just the illustrated preferred
5 embodiment, but is defined by the appended claims.

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WHAT IS CLAIMED IS:

1.   A CDMA communication system, in which bit rates
are dynamically allocated, comprising:

         a plurality of CDMA transmitting stations and a
single CDMA receiving station, all of which are
5   intercoupled to each other over a CDMA channel and a
feedback channel;

         each CDMA transmitting station including a
control circuit which sends control signals on said CDMA
channel in spaced apart time intervals which request
10 respective bit rates on said CDMA channel;

         said CDMA receiving station including a bit rate
allocating circuit which receives and responds to said
control signals by sending feedback messages over said
feedback channel that address individual CDMA transmitting
15 stations and grant respective bit rates to the addressed
station; and,

         each CDMA transmitting station including a
receiver circuit that receives those feedback messages
which address that particular station, and a data
20 transmitting circuit which sends CDMA digital data on said
CDMA channel at the bit rates granted in the received
feedback messages.

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2.   A CDMA communication system according to claim 1
wherein each of said transmitting stations includes a data
buffer which stores a time varying number of data bytes
that are to be sent, and said control circuit in each
transmitting station requests said respective bit rates by
including said number in said control signals.

3.   A CDMA communication system according to claim 1
wherein each of said transmitting stations includes a data
buffer which stores a time varying number of data bytes
that are to be sent, and said control circuit in each
transmitting station requests said respective bit rates by
including in said control signals the net variance in said
number between successive control signals.

4.   A CDMA communication system according to claim 1
wherein said data transmitting circuit, in each CDMA
transmitting station, modulates said data with a spreading
code at a fixed number of chips per second and a selectable
number of chips per bit in response to said granted bit
rate.

5.   A CDMA communication system according to claim 1
wherein each CDMA transmitting station modulates said
control signals and said digital data signals with a single
spreading code but in different time intervals which are
interleaved on said CDMA channel.

6.   A CDMA communication system according to claim 1
wherein each CDMA transmitting station modulates said
control signals and said digital data signals at the same
time but with different spreading codes on said CDMA
channel.

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7.   A CDMA communication system according to claim 1
wherein said bit rate allocating circuit tallies the bit
rates which it grants in said feedback messages, and
maintains the tally below a predetermined maximum aggregate
5 bit rate for said CDMA channel.

8.   A CDMA communication system according to claim 1
wherein said bit rate allocating circuit responds to said
control signals from one of said CDMA transmitting station
by sending a feedback message to a different CDMA
5 transmitting station which reduce that station's current
bit rate, and by thereafter sending another feedback
message to said one CDMA transmitting station which
increases that station's current bit rate.

9.   A CDMA communication system according to claim 1
wherein said CDMA channel and said feedback channel are in
a single coaxial cable.

10.   A CDMA communication system according to claim 1
wherein said CDMA channel and said feedback channel are in
a single hybrid optical fiber-coaxial cable transmission
medium.

11.   A CDMA communication system according to claim 1
wherein said CDMA channel and said feedback channel are in
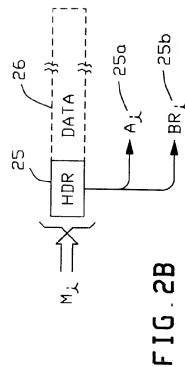a wireless transmission medium.
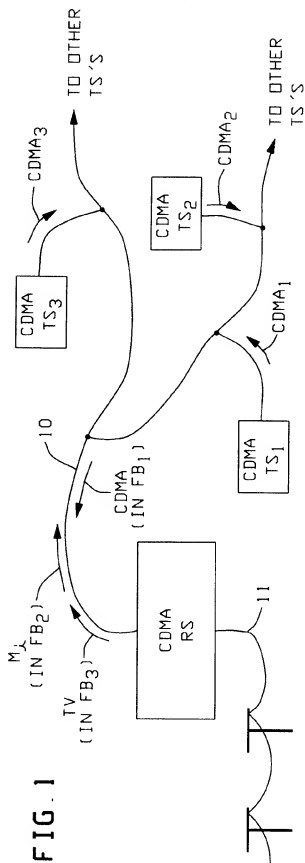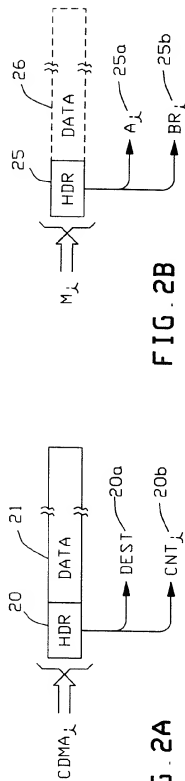
FIG. 1

FIG. 2A

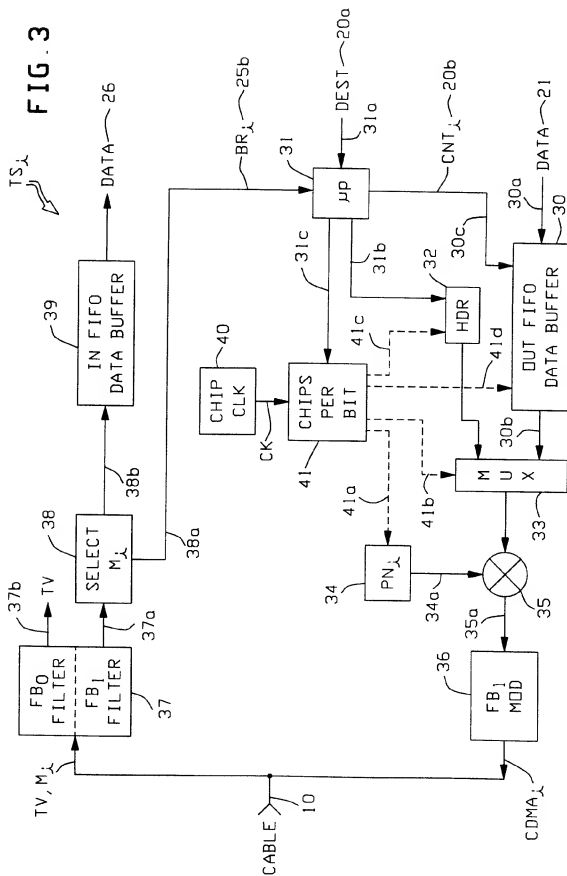FIG. 2B

FIG. 3
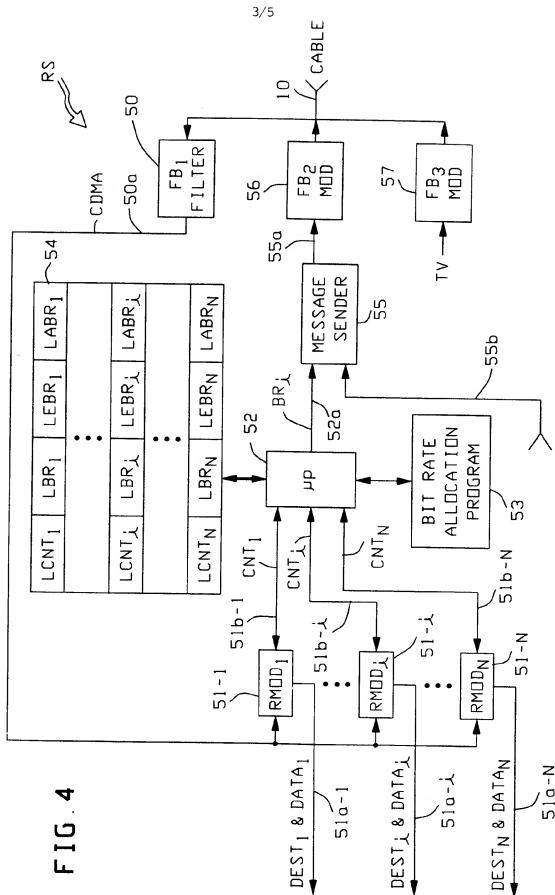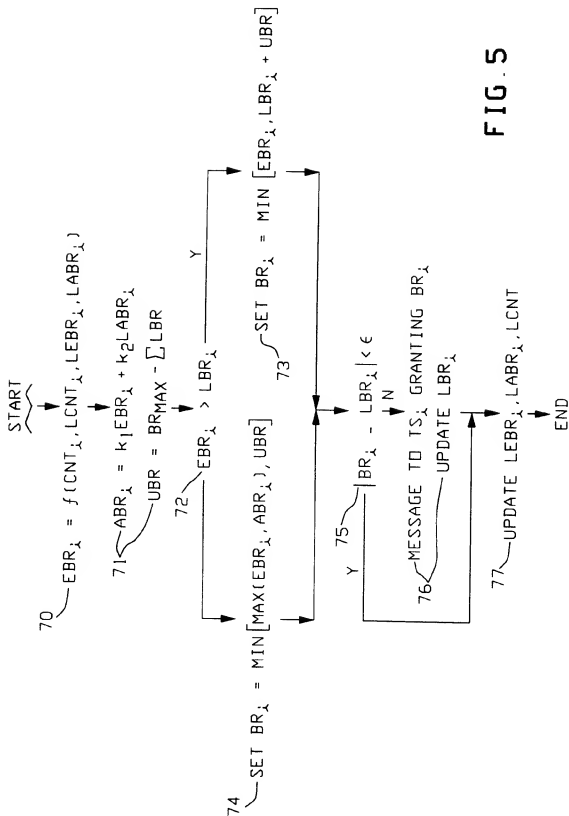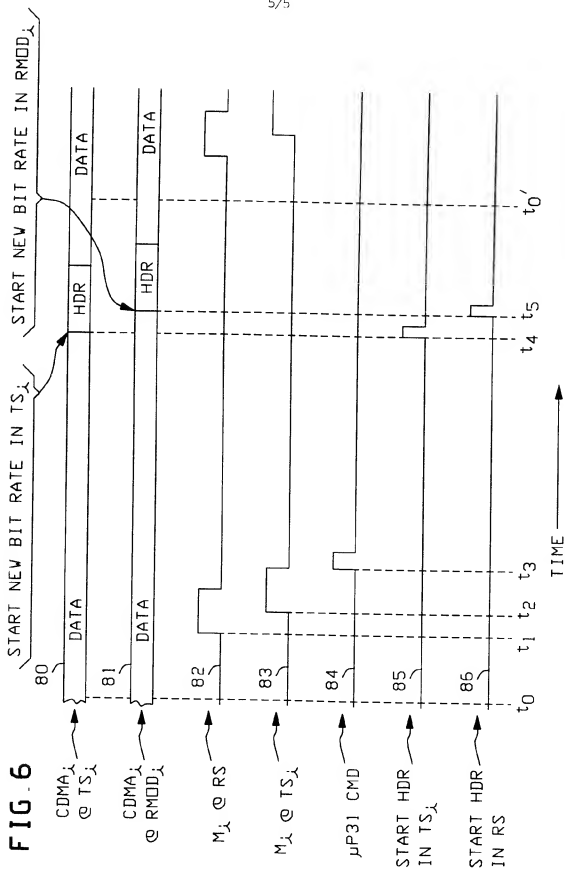
FIG. 4

START

70 — $EBR_i = f(CNT_i, LCNT_i, LEBR_i, LABR_i)$

71 — $ABR_i = k_1 EBR_i + k_2 LABR_i$

$UBR = BR_{MAX} - \sum LBR$

72 — $EBR_i > LBR_i$

Y → 73 — $SET\ BR_i = MIN\ [EBR_i, LBR_i + UBR]$

74 — $SET\ BR_i = MIN\ [MAX[EBR_i, ABR_i], UBR]$

75 — $|BR_i - LBR_i| < \epsilon$

Y

N

76 — MESSAGE TO TS$_i$ GRANTING BR_i

UPDATE LBR_i

77 — UPDATE $LEBR_i, LABR_i, LCNT$

END

FIG. 5

FIG. 6

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6   H04J13/00   H04B7/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6   H04J   H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category°	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A,5 128 959 (BRUCKERT EUGENE J) 7 July 1992	1,9-11
Y	see column 3, line 43 - line 59 see column 4, line 38 - line 58 see column 6, line 19 - line 45 see figure 3	5,7,8

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[X] Further documents are listed in the continuation of box C.   [X] Patent family members are listed in annex.

Date of the actual completion of the international search	Date of mailing of the international search report
17 October 1996	3 1. 10. 96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Pieper, T

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATION, vol. 12, no. 4, 1 May 1994, NEW YORK US, pages 733-743, XP000572845 BAIER A ET AL: "DESIGN STUDY FOR A CDMA-BASED THIRD-GENERATION MOBILE RADIO SYSTEM"	1,6,11
A	see page 634, left-hand column, line 13 - line 29 see page 734, right-hand column, line 10 - page 735, left-hand column, line 24 see page 735, left-hand column, line 42 - right-hand column, line 12 see page 736, right-hand column, line 4 - line 17 see page 737, right-hand column, paragraph 3 ---	4,7,8
Y	IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATIONS, JUNE 1994, USA, vol. 12, no. 5, June 1994, ISSN 0733-8716, pages 900-908, XP000464975 MCTIFFIN M J ET AL: "Mobile access to an ATM network using a CDMA air interface" see page 901, right-hand column, last paragraph - page 902, left-hand column, paragraph 1 see page 904, right-hand column, last paragraph - page 905, left-hand column, paragraph 2 ---	5
Y	SERVING HUMANITY THROUGH COMMUNICATIONS. SUPERCOMM/ICC, NEW ORLEANS, MAY 1 - 5, 1994, vol. VOL. 2, no. -, 1 May 1994, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 1104-1110, XP000438672 NING GUO ET AL: "NETWORKS THE GRADE OF SERVICE FOR INTEGRATED VOICE/DATA WIRELESS DS-CDMA" see page 1107, left-hand column, paragraph 4 - last paragraph see page 1108, right-hand column, paragraph 2 - page 1109, left-hand column, paragraph 1 ---	7,8
A	US,A,5 373 502 (TURBAN KARL-ALBERT) 13 December 1994 see column 4, line 15 - line 22 see column 4, line 39 - line 43 see column 4, line 61 - line 65 see column 6, line 29 - line 31 see column 8, line 28 - line 44 see column 8, line 57 - line 62 ---	1-3,5,6, 9-11

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO,A,95 10145 (NOKIA TELECOMMUNICATIONS OY ;KESKITALO ILKKA (FI); KIEMA ARTO (FI)) 13 April 1995 see page 4, line 13 - page 5, line 7 see page 7, line 23 - line 35 ---	4
A	OFC '95 OPTICAL FIBER COMMUNICATION. SUMMARIES OF PAPERS PRESENTED AT THE CONFERENCE ON OPTICAL FIBER COMMUNICATION. VOL.8. 1995 TECHNICAL DIGEST SERIES. POSTCONFERENCE EDITION, OFC '95 OPTICAL FIBER COMMUNICATION. SUMMARIES OF PAPERS PRESENTED AT TH, ISBN 0-7803-2654-7, 1995, WASHINGTON, DC, USA, OPT. SOC. AMERICA, USA, page 53 XP002016264 ELDERING C A ET AL: "Performance comparison of multiple-access techniques in hybrid fiber-coax return systems" see page 53, left-hand column, paragraph 1 -----	10

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